High·performance·PWM·Power·Switch IC

1. Feature

Meet DoE VI and CoC V5 energy efficiency requirements
No load standby power consumption as low as 50 mW
Precision programmable output overvoltage protection (TrueOVP™)
Built-in oscillator with maximum 65 kHz frequency limit
Built-in soft start control circuit reduces switch impact
Built-in second-generation C.T.™ technology optimizes EMI performance
Extended mode light load control for optimized efficiency and light load power
Full range of no audio noise working methods
Integrated synchronous current ramp compensation
VDD overvoltage clamp and undervoltage lockout (UVLO)
Gate drive output voltage smart clamp function
Built-in input line voltage compensation
Built-in programmable input undervoltage protection (ACUVP)
Cycle-by-Cycle Current Limiting with Leading Edge Blanking (OCP)
Output overcurrent, overload, short circuit protection (OLP)
Wide voltage output power up to 25W, peak power is 30W
Available in a highly isolation SOP8/DIP7 package

2. Applications

Power Adapter
Battery Charger
Set-top box Power
Open-frame Power

3. Description

The LN9T26 is a high performance, highly integrated current mode PWM controller that makes it easy to build low standby power, low cost, high performance solutions to meet CoC V5 and DoE VI energy efficiency in applications. The PWM switching frequency is internally set by the chip and has full temperature compensation. The maximum value is set at 65 kHz. Under no-load or light load conditions, the IC can operate in intelligent interrupt mode to reduce switching losses, so it can be achieved good conversion efficiency while having lower standby power consumption. The low VDD startup current and operating current allow the LN9T26 to have very high reliability and longevity. A resistor with larger resistance can be used to complete the circuit startup, which also reduces the loss of the startup resistor, further reduces the system standby power. The built-in current ramp compensation greatly optimizes the reliability of the circuit over large PWM duty cycles and avoids subharmonic oscillations that may occur. The built-in leading edge blanking circuit avoids the inductance turn-on current spike interference with current sampling and the effect on the snubber diode reverse recovery current, and the external no

longer requires an additional blanking circuit.The LN9T26 also offers a very comprehensive protection circuit with auto-recovery, including cycle-by-cycle current limit (OCP), output overload protection (OLP) with high and low voltage compensation, VDD overvoltage protection and undervoltage lockout (UVLO), the output overvoltage precision protection function (TrueOVP™) and the input undervoltage protection function (ACUVP) when the feedback is open can be set externally. The voltage at the drive output is automatically limited to no more than 15 V to protect the MOSFET from safety.

Based on the new smartEnergy™ technology from Lii Semi, the system standby power and light load efficiency are greatly improved. The conversion efficiency can meet the CoC and DoE VI energy efficiency requirements in general application, and the no-load power can be as low as 50 mW or less.

By incorporating the unique second-generation C.T.™ patented technology from Lii Semi into the output pulse with specially designed output soft clamp totem pole technology, the EMI characteristics of the system have been greatly improved and can easily meet the electromagnetic compatibility standards of various countries.

Highly isolated standard SOP8/DIP7 green packages are available.

4. Functional Block Diagram

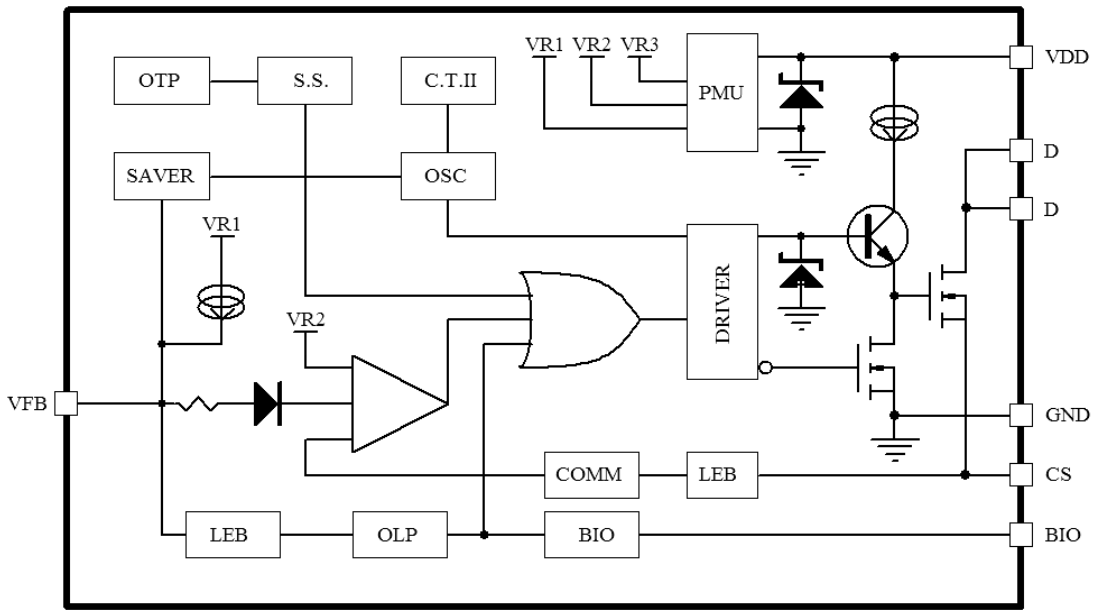

Fig1. Internal functional block diagram

5. Pin Definitions

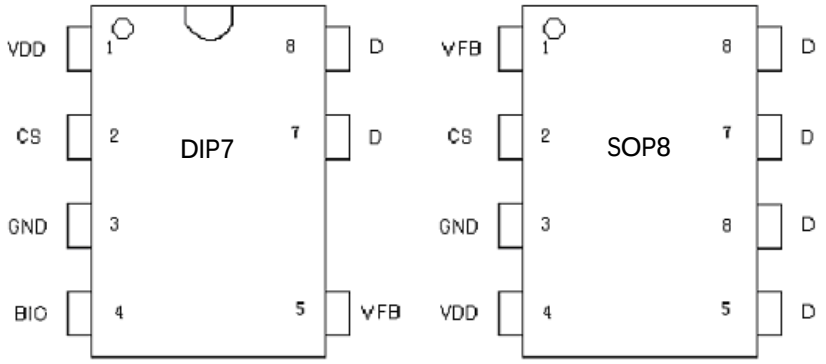

Fig2. Pin Definitions

6. Pin Function Description

DIP7	SOP8	Symbol	Function
1	4	VDD	Power supply pin, connect the starting resistor and auxiliary power supply circuit
2	2	CS	Switch current sense signal input pin, connected to the current limit resistor
3	3	GND	Ground pin
4	/	BIO	Output OVP and input UVP detection pin, connect the set resistor
5	1	VFB	Feedback signal input pin, connected to output feedback signal (optocoupler)
7,8	5,6,7,8	D	The high-voltage MOSFET switch's drain pin, which connects the transformer primary winding

7. Typical Simplified Schematic

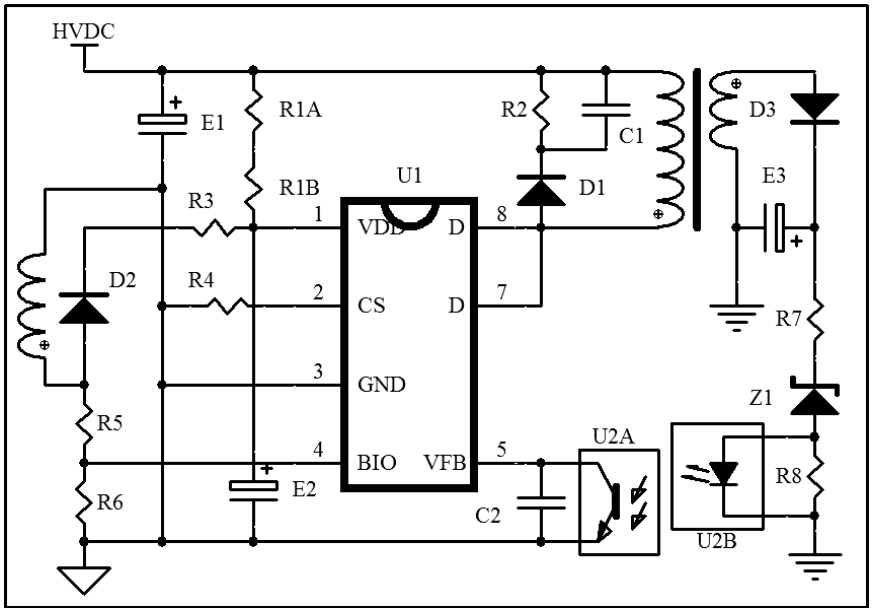

Fig3. Typical Simplified Schematic

8. Absolute Maximum Ratings *

Parameter		Rating	Units
D Pin Voltage		650**	V
D Pin Input Current		4***	A
VDD Pin Voltage		30**	V
Other Pin Voltage		-0.3 to +7	V
PD		1500	mW
Min/Max Operating Junction Temperature T_J		-40 to +150	℃
Min/Max Operating Ambient Temperature Ta		-20 to +105	℃
Min/Max Storage Temperature Tstg		-55 to +150	℃
Recommended Soldering Conditions		260℃，10S	
ESD	HBM	2500	V
	MM	250	V

Note*: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for ex tended periods may affect device reliability. ** : With 10 mA limit. ***: Only allow 1 ms pulse and period is 1 s.

9. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VDD	VDD Supply Voltage	10		25	V
Vds	Drain Peak Voltage	-	-	650	V
Ids	Drain Peak Current	-	-	1.5	A
TA	Operating Ambient Temperature	-20	-	85	℃

10. Electrical Characteristics(Ta = 25℃, VDD=15V, if not otherwise noted)

MOSFET Section (Drain Pin)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Voltage	VDD=0 V, I_D=1 mA	650	700	-	V
I_{HV}	D-S Leakage Current	V_D=650 V	-	-	10	uA
V_{DSON}	Voltage at RdsON	I_D=1.5 A, T_J=25 ℃	-	3.5	-	V
T_R	Switch Rise Time	CL=1 mH	-	35	-	nS
T_F	Switch Fall Time	CL=1 mH	-	35	-	nS
I_D	Drain Current Pulsed	T_J=25 ℃	-	4	-	A
		T_J=125 ℃	-	2	-	A

VDD Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{QS}	VDD Startup Current	VDD=14 V	-	1	10	uA
I_Q	Operating Current	VDD=16 V,VFB=OPEN	-	1.2	-	mA
V_{STOP}	UVLO Threshold Voltage	FB=0	7.8	8.8	9.8	V
V_{START}			-	21	-	V
V_{OVP}	VDD OVP Threshold		-	28	-	V
VDD_CL	VDD Clamp Voltage	I_{VDD}=10 mA	-	30	-	V

VFB Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{FB}	VFB Open Loop Voltage	V_{FB} is open		4.6		V
I_{FB_S}	FB Short Circuit Current	FB=0		0.27		mA
VTH_{MIN}	Zero Duty Cycle Threshold Voltage	VDD=16 V		0.75		V
VTH_{MAX}	Power Limit Threshold Voltage	VDD=16 V		3.7		V
T_{OLPI}	Power Limit Delay Time	VDD=16 V		85		mS
D_{MAX}	Max. Duty Cycle	VDD=16 V, FB=3.3 V, CS=0		80		%

CS Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
T_{LEB}	L.E.B Time		-	250	-	nS
Z_{CS}	CS Input Resistance		-	40	-	KΩ
T_{OCP}	OCP Delay Time	VDD=16 V, V_{CS}>VTH_OC, FB=3.3 V	-	75	-	nS
VTH_{OCP}	Max. CS Threshold	FB=3.3V	-	0.75	-	V
T_{SS}	Internal Soft Start Delay		-	12	-	mS
VTH_{OSP}	OSP Threshold Voltage		-	1.45	-	V

OSC Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{OSC}	Switching Frequency		60	65	70	kHz
ΔF_{OSC}_T	F_{OSC} VS Ta	VDD=16 V, Ta=-20 ℃ to 100 ℃	-	5	-	%
ΔF_{OSC}_V	F_{OSC} VS VCC	VDD=12-25 V	-	5	-	%
F_{OSC_MIN}	Min. Burst Mode frequency	VDD=16 V	-	22	-	kHz

Cycleturning™II (C.T.II) Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ΔF_{OSC}	C.T. Range		-	±4	-	%
T_{CT}	C.T. Time		-	4	-	mS

BIO Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{BIO}	BIO Pull-up Current	VDD = 16V		0.27		mA
V_{OVP}	Overvoltage Protection Threshold	VDD = 16V		3.0		V
T_{OVP}	Overvoltage Protection Delay	VDD = 16V		3		us
V_{UVP}	Undervoltage Protection Threshold	VDD = 16V		3.0		V
T_{UVP}	Undervoltage Protection Delay	VDD = 16V		65		ms

Thermal Data

Symbol	Parameter	Rating	Unit
θ_{JA}[1]	Thermal Resistance Junction-Ambient	60	℃/W
θ_{JC}[2]	Thermal Resistance Junction-Case	15（DIP7）/25(SOP8)	℃/W

Notes: 1. All leads are soldered on a 250 mm^2 copper foil with 2 oz thick to measuring. 2. Measured on the surface of the package near pin 7.

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12. Application and Implementation

The LN9T26 is a highly integrated PWM control IC that is optimized for 25 W off-line applications. Its high-efficiency Burst mode control greatly reduces standby loss, improves conversion efficiency at light loads, and easily meets international energy efficiency standards such as CoC V5 and DoE VI.

12.1 Start-up current and start-up control

The LN9T26 can operate at very low start-up current conditions, with accurate UVLO control enabling fast and reliable power-up in a short period of time. Allowing a large start-up resistor value can significantly reduce the start-up power consumption, such as 3 MΩ, although a 1/8W power-class resistor can meet the required power requirements, but must still carefully consider its ability to withstand voltage, The use of resistors in series is recommended, for example, using two 1206-type chip resistors in series.

The start-up resistor can be connected between AC input terminal or the positive of input DC high voltage and the VDD storage capacitor.

12.2 Operating current and VDD capacitance

The normal operating current of LN9T26 is as low as 1.2 mA. The loss of the IC itself is small during operation. An electrolytic capacitor with capacity of not less than 4.7 uF can meet the sufficient energy required for IC power supply and driving, but consider the larger input capacitance of MOSFET and the wider operating temperature range, a lower internal resistance (ESR) type of the capacitor should be chosen to provide fast and large current when the MOSFET is turned on, speeding up MOSFET turn-on.

12.3 Cycleturning™ II (C.T. II)

The LN9T26 integrates the optimized second-generation Cycleturning™ proprietary technology from the clock cycle is modulated at the set time in the work process, resulting in a larger switching pulse spectrum to reduce the narrowband energy density, so that the average interference intensity in any single bandwidth is greatly reduced. Therefore, the cost of the system on EMI is also greatly reduced.

12.4 Extended BM operating characteristics

Under no-load or light-load conditions, the ratio of the total loss of MOSFET switching losses will increase significantly, and the switching loss is proportional to the switching frequency. Lowering the switching frequency can significantly reduce the switching losses of the MOSFET. LN9T26 by detecting the FB voltage and time size, the system no-load or light load will automatically adjust the switching frequency to a lower value, the more FB voltage is lower than the set control voltage, the more the frequency decreases, but the circuit automatically limits the minimum value of the frequency drop above 22 kHz to avoid audible noise.

When the system frequency drops to near 22 kHz, if the FB voltage is still lower than the set threshold voltage, the output will be disabled to ensure that the output voltage will not be too high.

12.5 Current detection and leading edge blanking

The LN9T26 provides cycle-by-cycle current limiting, and the switching current is sampled into the IC through the current limiting resistor. The built-in leading-edge blanking eliminates current spikes into the IC, avoid the current limit function malfunction, the MOSFET will not be turned off by mistake, so the traditional external blanking circuits will no longer be needed.

The duty cycle of the PWM is determined by the combination of the sampling current and the FB voltage. The typical threshold voltage of the overcurrent comparator when FB is floating is 0.75 V.

12.6 Synchronous slope compensation

The IC integrates a voltage slope that is synchronized with the clock to the compensation circuit of the current sampling signal, which greatly improves the infinite loop stability of the circuit at large duty cycles and CCM, prevents possible subharmonic oscillation problems, and enhances output voltage stability.

12.7 Output power switch

The LN9T26 integrates a MOSFET power switch BVdss voltage up to 650 V. The power switch has extremely low RdsON internal resistance and extremely high switching speed. It can maintain extremely low switching loss at switching frequency up to 65 kHz. Excellent electrical performance ensures the performance characteristics of the chip and has a very high reliability.

12.8 Protective function

Excellent power systems require sophisticated fault protection to achieve high reliability. The LN9T26 is designed with a wide range of protection features to meet user requirements including cycle-by-cycle current limiting (OCP), output overload protection (OLP), VDD overvoltage lockout, and under-voltage lockout (UVLO).

With built-in input voltage compensation technology, the output power is limited to a relatively constant value, which makes the selection of the output rectifier device very easy, and the output diode specifications can be selected more economically to meet a relatively constant output over-current at wide input voltage conditions results in lower system cost.

When the output is overloaded, the FB voltage rises and reaches the set TD_PL value, the circuit will turn off the MOSFET output, and the system will restart when the VDD voltage drops to the UVLO set point. If the fault does not cancel, the circuit will enter the hiccup protection mode.

The specially designed BIO pin allows you to accurately set the maximum output voltage parameter under feedback loop fault conditions by simply sampling the voltage waveform from the auxiliary winding. This makes it easy to meet the most demanding output overvoltage protection requirements.

The resistor network connected to the BIO pin also sends the input voltage to the internal under-voltage protection circuit during startup to disable the system startup when the input voltage is too low, thus avoiding output voltage jumps caused by excessive low voltage conditions or the system constantly trying to start up when the system is turned off.

After normal operation, VDD is powered by the auxiliary winding of the transformer. If the voltage exceeds the limit voltage, it will be clamped. When the voltage is lower than the UVLO setting voltage, the circuit output will be turned off and the

system will be restarted.

13. Layout Guidelines

13.1 Principles of high-frequency layout

When switching power supply layout should follow the principle of high-frequency layout, where possible, the current loop should be kept to a minimum. It should be advanced and then out of the dual-capacitor and appropriate to maintain a single point of connection capacitance. Three typical current loops are shown in the following figure:

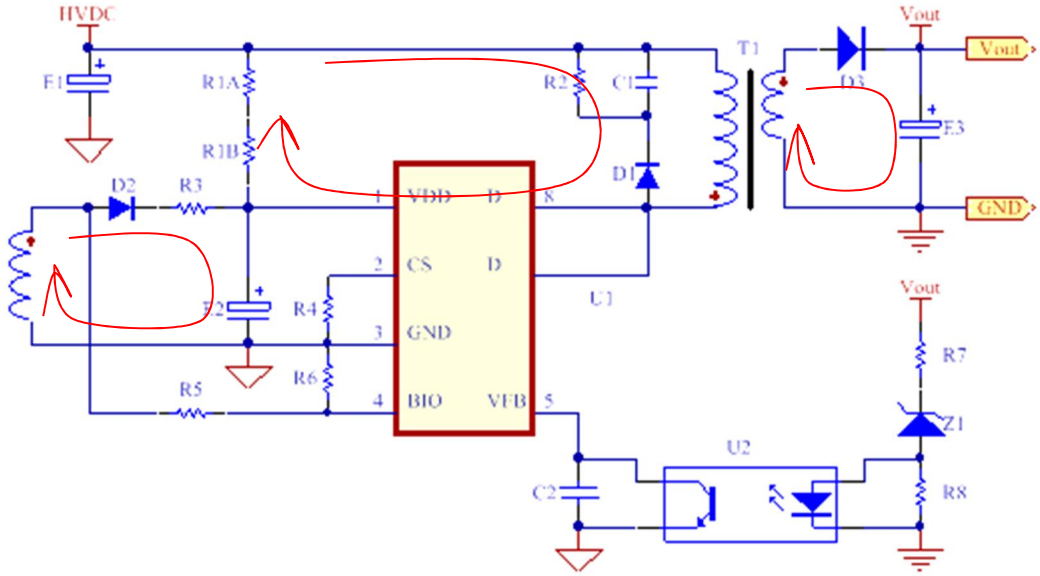


Fig4. Typical current loop diagram

13.2 Typical layout reference

An example of a typical PCB layout is shown below.

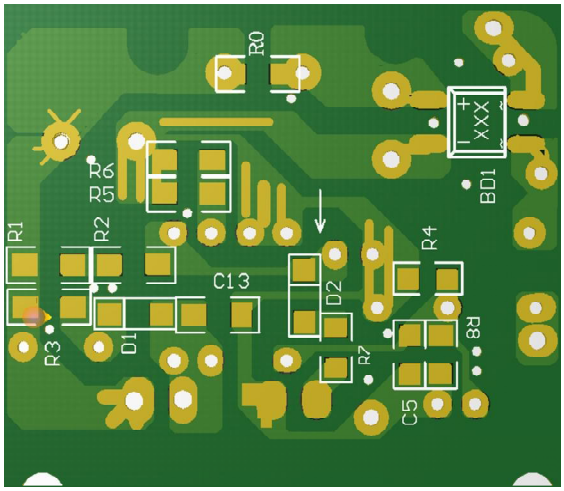


Fig5. Typical layout reference (bottom view)

14. Typical Application Circuit Schematic（input：90~265 Vac）

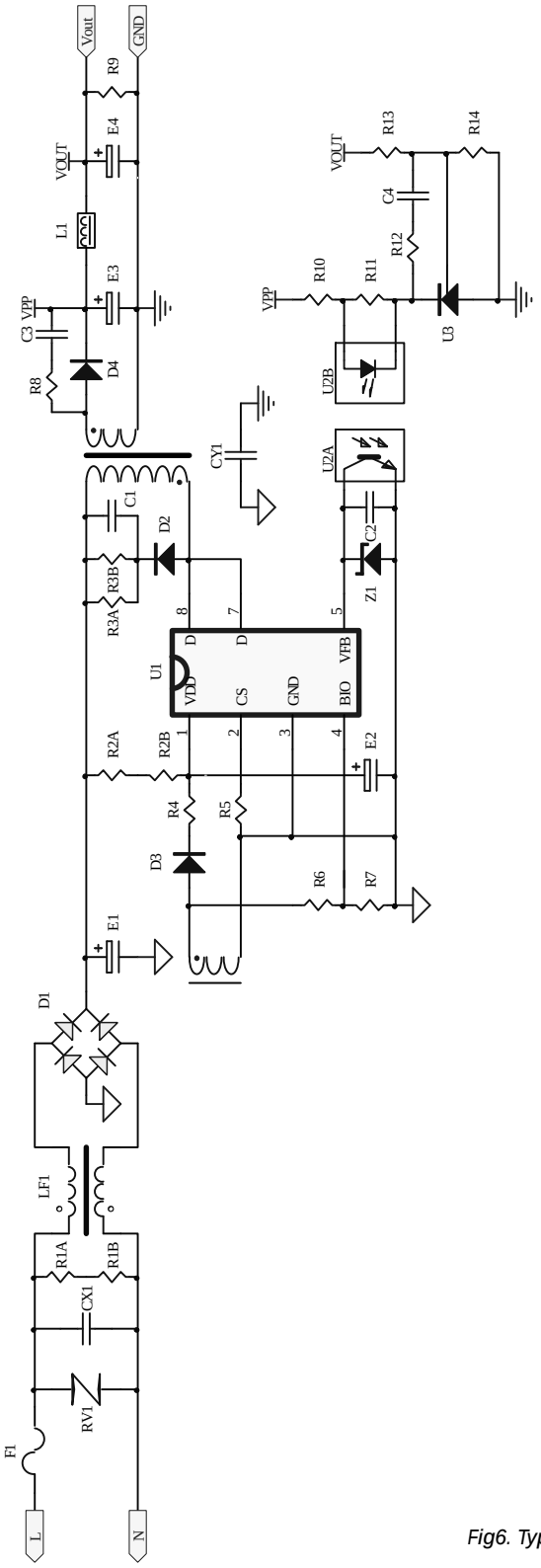
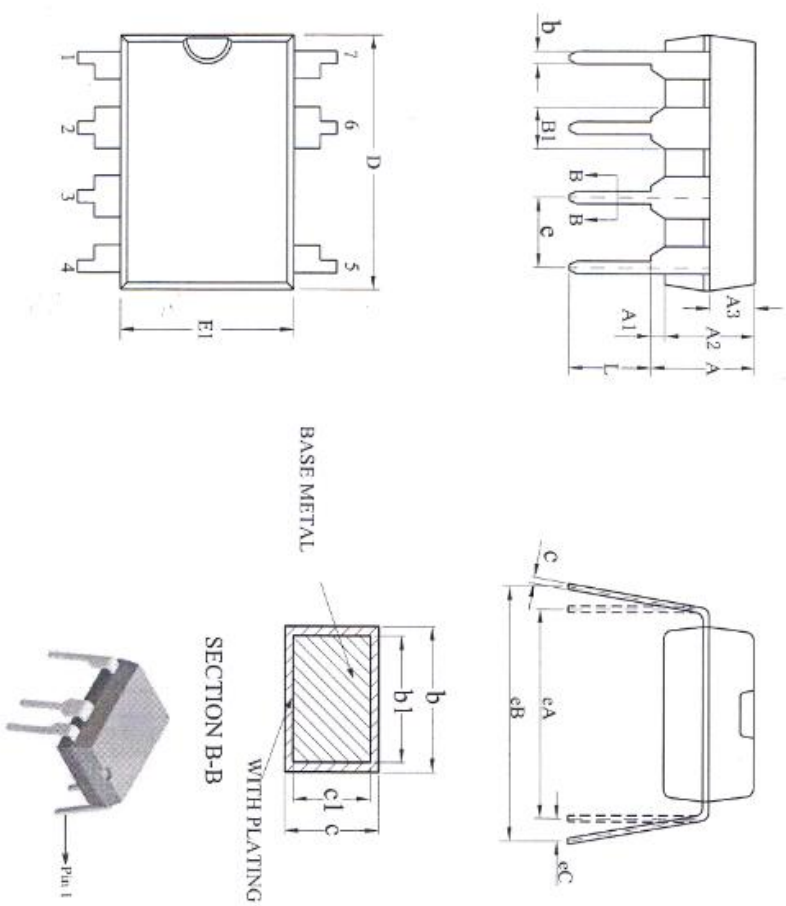


Fig6. Typical Application Circuit Schematic

15. Mechanical and Packaging

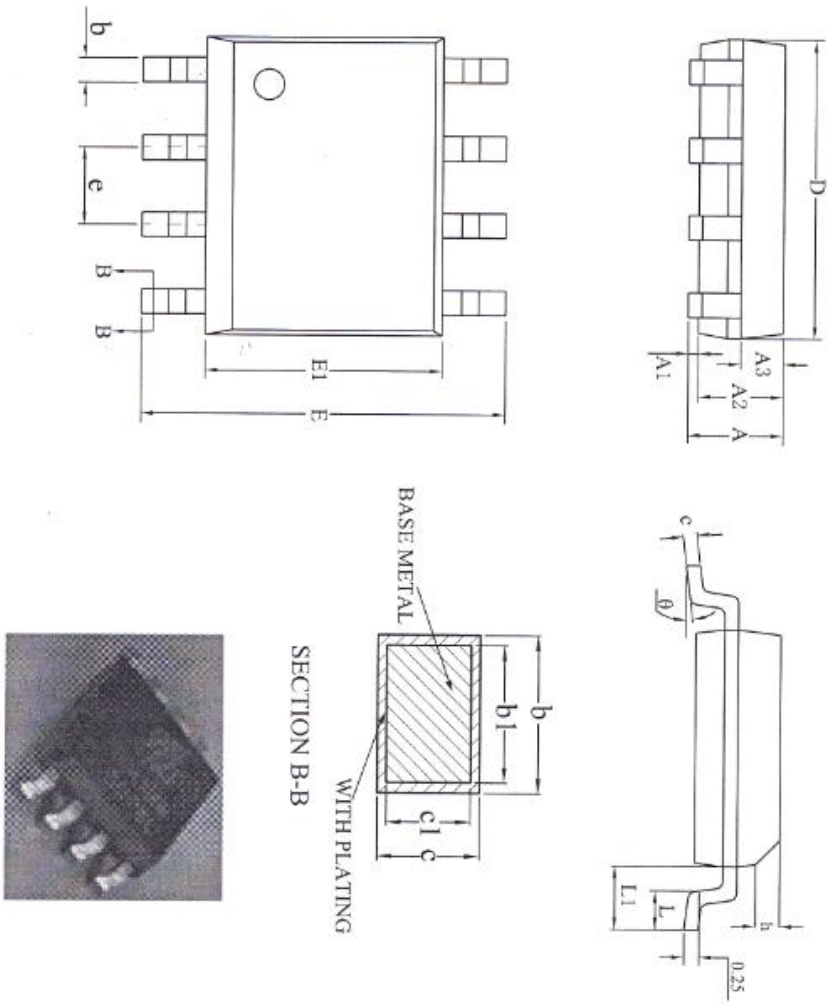
DIP7



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	—	—
A2	3.20	3.30	3.40
A3	1.55	1.60	1.65
b	0.44	—	0.52
b1	0.43	0.46	0.49
B1	1.52REF		
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	9.15	9.25	9.35
E1	6.25	6.35	6.45
e	2.54BSC		
eA	7.62REF		
eB	7.62	—	9.30
eC	0	—	0.84
L	3.00	—	—

Fig7. Mechanical Dimensional Drawings(mm)1

SOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Fig7. Mechanical Dimensional Drawings(mm)2

16. Orderable Information

Part No.	Green Standard	Switch frequency	Package	Quantity per Tube
LN9T26	RoHs	65 kHz	DIP7	50 PCS/TUBE
LN9T26	RoHs	65 kHz	SOP8	100 PCS/TUBE

17. Important Notice

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